

DERWENT- 1997-003674  
ACC-NO:

DERWENT- 199701  
WEEK:

*COPYRIGHT 1999 DERWENT INFORMATION LTD*

TITLE: Trouble processing method for parallel processor - involves judging abnormality in reception of data packet, when received start and end codes are not in agreement with start and end codes held by reception side processor

PRIORITY-DATA: 1995JP-0075007 (March 31, 1995)

PATENT-FAMILY:

| PUB-NO        | PUB-DATE         | LANGUAGE | PAGES | MAIN-IPC    |
|---------------|------------------|----------|-------|-------------|
| JP 08272752 A | October 18, 1996 | N/A      | 018   | G06F 015/16 |

INT-CL (IPC): G06F015/16

ABSTRACTED-PUB-NO: JP 08272752A

BASIC-ABSTRACT:

The method is applied to multiple parallel processors (PU-0 - PU-n) which are connected through a network (NW). A transmission side processor transfers a start code (SF) that indicates the commencement of packet transfer, before the actual starting of packet transfer operation. An end code indicating the completion of data transfer is transmitted by the transmission side processor, after the last data packet is transmitted. The reception side processor also holds the start and end codes.

A judgment unit judges abnormality in the reception of packet, when the received start code and the end code are not in agreement with the start code to the end code held by the reception side processor. A dummy data transmission is carried out by the transmission side processor during the time of main memory disorder. In this situation, the reception side processor inhibits storage of the data received with a superscript indicating that the data is a dummy data.

ADVANTAGE - Detects packet data length error or packet loss, correctly. Prevents system crash due to network path blockade between processors.

---

Derwent Accession Number - NRAN (1):

1997-003674

Title - TIX (1):

Trouble processing method for parallel processor - involves judging

abnormality in reception of data packet, when received start and end codes are not in agreement with start and end codes held by reception side processor